In The Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (canceled)

2. (currently amended) ~~An electronic device according to Claim 1~~ An electronic device comprising:

a first integrated circuit substrate;

a second integrated circuit substrate on the first integrated circuit substrate;

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;

a first electrical and mechanical connection between the first and third integrated circuit substrates wherein the first electrical and mechanical connection bypasses the second integrated circuit substrate;

a second electrical and mechanical connection between the second and third integrated circuit substrates; and

a third electrical and mechanical connection between the first and second integrated circuit substrates;

wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond an end of the second integrated circuit substrate.

3. (previously presented) An electronic device according to Claim 2 wherein the first electrical and mechanical connection is between portions of the first and third integrated circuit substrates extending beyond the end of the second integrated circuit substrate.

4. (previously presented) An electronic device according to Claim 3 further comprising:

a conductive trace on a surface of the third integrated circuit substrate, the conductive trace providing an electrical coupling between the first and second electrical and mechanical connections.

5. (canceled).

6. (currently amended) ~~An electronic device according to Claim 1 further comprising:~~ An electronic device comprising:

a first integrated circuit substrate;

a second integrated circuit substrate on the first integrated circuit substrate;

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;

a first electrical and mechanical connection between the first and third integrated circuit substrates wherein the first electrical and mechanical connection bypasses the second integrated circuit substrate;

a second electrical and mechanical connection between the second and third integrated circuit substrates;

a third electrical and mechanical connection between the first and second integrated circuit substrates; and

a conductive trace on a surface of the first integrated circuit substrate, the conductive trace providing an electrical coupling between the first and third electrical and mechanical connections.

7. (currently amended) ~~An electronic device according to Claim 1~~ An electronic device comprising:

a first integrated circuit substrate;

a second integrated circuit substrate on the first integrated circuit substrate;

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;

a first electrical and mechanical connection between the first and third integrated circuit substrates wherein the first electrical and mechanical connection bypasses the second integrated circuit substrate;

a second electrical and mechanical connection between the second and third integrated circuit substrates; and

a third electrical and mechanical connection between the first and second integrated circuit substrates;

wherein the first electrical and mechanical connection comprises a first conductive bump between the first and third integrated circuit substrates, wherein the first conductive bump is spaced apart from and extends past an edge of the second integrated circuit substrate, and wherein the second electrical and mechanical connection comprises a second conductive bump between the second and third integrated circuit substrates.

8. (original) An electronic device according to Claim 7 wherein the first conductive bump has a greater volume than the second conductive bump.

9. (previously presented) An electronic device comprising:

a first integrated circuit substrate;

a second integrated circuit substrate on the first integrated circuit substrate;

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;

a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump is spaced apart from and extends past an edge of the

second integrated circuit substrate wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates; and

a second conductive bump between the second and third integrated circuit substrates wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates;

wherein each of the first, second, and third integrated circuit substrates includes a device side having electronic circuits thereon and a backside, wherein the device sides of the first, second, and third integrated circuit substrates face a first direction, and the backsides of the first, second, and third integrated circuit substrates face a second direction.

10. (previously presented) An electronic device according to Claim 9 wherein both of the first and third integrated circuit substrates are integrated circuit memory devices.

11. (previously presented) An electronic device according to Claim 10 wherein both of the first and second conductive bumps are electrically coupled to a data input, a data output, and/or an address input of the third integrated circuit substrate.

12. (previously presented) An electronic device according to Claim 11 wherein the second integrated circuit substrate is an integrated circuit memory device.

13. (previously presented) An electronic device according to Claim 12 wherein both of the first and second conductive bumps are electrically coupled to a data input, a data output, and/or an address input of the second integrated circuit substrate, and to a data input, a data output, and/or an address input of the first integrated circuit substrate.

14. (previously presented) An electronic device according to Claim 10 wherein the first and third integrated circuit substrates comprise memory devices having a same layout.

15. (previously presented) An electronic device comprising:

a first integrated circuit substrate;

a second integrated circuit substrate on the first integrated circuit substrate;

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;

a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump is spaced apart from and extends past an edge of the second integrated circuit substrate wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates;

a second conductive bump between the second and third integrated circuit substrates wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates;

a printed circuit board, wherein the first, second, and third integrated circuit substrates have device sides facing the printed circuit board and backsides facing away from the printed circuit board;

a third conductive bump between the first integrated circuit substrate and the printed circuit board wherein the third conductive bump provides electrical and mechanical connection between the first integrated circuit substrate and the printed circuit board;

a fourth conductive bump between the second integrated circuit substrate and the printed circuit board wherein the fourth conductive bump provides electrical and mechanical connection between the second integrated circuit substrate and the printed circuit board; and

a fifth conductive bump between the second integrated circuit substrate and the first integrated circuit substrate wherein the fifth conductive bump provides electrical and mechanical connection between the first and second integrated circuit substrates.

16. (previously presented) An electronic device according to Claim 15 wherein the printed circuit board includes a first conductive pad to which the third conductive bump is bonded and a second conductive pad to which the fourth conductive bump is bonded, wherein the first conductive pad has a greater surface area than the second conductive pad.

17. (previously presented) An electronic device according to Claim 15 further comprising:

a first conductive trace on the printed circuit board providing electrical coupling between the third and fourth conductive bumps;

a second conductive trace on the second integrated circuit substrate providing electrical coupling between the fourth and fifth conductive bumps; and

a third conductive trace on the first substrate providing electrical coupling between the fifth and first conductive bumps.

18. (previously presented) An electronic device according to Claim 17 wherein the first and third conductive bumps are electrically coupled to a data input, a data output, and/or an address input of the first integrated circuit substrate, and wherein the first and third conductive bumps are electrically coupled to a data input, a data output, and/or an address input of the third integrated circuit substrate.

19. (previously presented) An electronic device comprising:

a first integrated circuit substrate;

a second integrated circuit substrate on the first integrated circuit substrate;

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;

a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump is spaced apart from and extends past an edge of the second integrated circuit substrate wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates;

a second conductive bump between the second and third integrated circuit substrates wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates;

a fourth integrated circuit substrate on the third integrated circuit substrate so that the third integrated circuit substrate is between the second and fourth integrated circuit substrates;

a fifth integrated circuit substrate on the fourth integrated circuit substrate so that the fourth integrated circuit substrate is between the third and fifth integrated circuit substrates;

a third conductive bump between the second and fourth integrated circuit substrates wherein the third conductive bump provides electrical and mechanical connection between the second and fourth integrated circuit substrates;

a fourth conductive bump between the fourth and third integrated circuit substrates wherein the fourth conductive bump provides electrical and mechanical connection between the fourth and third integrated circuit substrates; and

a fifth conductive bump between the third and fifth integrated circuit substrates wherein the fifth conductive bump provides electrical and mechanical connection between the third and fifth integrated circuit substrates;

wherein the first, second, third, fourth and fifth conductive bumps comprise portions of a signal path, wherein a direct electrical coupling is provided between the signal path and an electronic circuit of the fifth integrated circuit substrate, and wherein the signal path is free of a direct electrical coupling with any electronic circuit of the third integrated circuit substrate.

Claim 20 (canceled).

21. (previously presented) An electronic device comprising:

a printed circuit board;

a first integrated circuit substrate on the printed circuit board;

a second integrated circuit substrate on the first integrated circuit substrate wherein the first integrated circuit substrate is between the printed circuit board and the second integrated circuit substrate; and

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit

substrates, wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond a first end of the second integrated circuit substrate wherein a second end of the second integrated circuit substrate extends beyond the first and third integrated circuit substrates wherein each of the first, second, and third integrated circuit substrates is on a same side of the printed circuit board and wherein each of the first, second, and third integrated circuit substrates has a device side facing the printed circuit board and a backside facing away from the printed circuit board.

22. (previously presented) An electronic device comprising:

a printed circuit board;

a first integrated circuit substrate on the printed circuit board;

a second integrated circuit substrate on the first integrated circuit substrate wherein the first integrated circuit substrate is between the printed circuit board and the second integrated circuit substrate;

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond an end of the second integrated circuit substrate;

a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates; and

a second conductive bump between the second and third integrated circuit substrates wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates.

23. (previously presented) An electronic device according to Claim 22 wherein the first conductive bump is between portions of the first and third integrated circuit substrates

extending beyond the end of the second integrated circuit substrate.

24. (previously presented) An electronic device according to Claim 22 further comprising:

a conductive trace on a surface of the third integrated circuit substrate, the conductive trace providing an electrical coupling between the first and second conductive bumps.

25. (previously presented) An electronic device according to Claim 22 further comprising:

a third conductive bump between the first and second integrated circuit substrates.

26. (previously presented) An electronic device according to Claim 25 further comprising:

a conductive trace on a surface of the first integrated circuit substrate, the conductive trace providing an electrical coupling between the first and third conductive bumps.

27. (previously presented) An electronic device comprising:

a printed circuit board;

a first integrated circuit substrate on the printed circuit board;

a second integrated circuit substrate on the first integrated circuit substrate wherein the first integrated circuit substrate is between the printed circuit board and the second integrated circuit substrate;

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond an end of the second integrated circuit substrate;

a first conductive bump between the first and third integrated circuit substrates, wherein the first conductive bump provides electrical and mechanical connection between the

first and third integrated circuit substrates; and

a second conductive bump between the second and third integrated circuit substrates, wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates;

wherein the first, second, and third integrated circuit substrates have a same size.

28. (original) An electronic device according to Claim 27 wherein the first conductive bump has a greater volume than the second conductive bump.

29. (previously presented) An electronic device comprising:

a printed circuit board;

a first integrated circuit substrate on the printed circuit board;

a second integrated circuit substrate on the first integrated circuit substrate wherein the first integrated circuit substrate is between the printed circuit board and the second integrated circuit substrate; and

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond an end of the second integrated circuit substrate;

wherein each of the first, second, and third integrated circuit substrates includes a device side having electronic circuits thereon and a backside, wherein each of the first, second, and third integrated circuit substrates is on a same side of the printed circuit board and wherein the device side of each of the first, second, and third integrated circuit substrates faces the printed circuit board and the backside of each of the first, second, and third integrated circuit electronic devices faces away from the printed circuit board.

30. (previously presented) An electronic device according to Claim 29 wherein each of the first, second, and third integrated circuit substrates are integrated circuit memory

devices.

31. (previously presented) An electronic device according to Claim 30 further comprising:

a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates; and

a second conductive bump between the second and third integrated circuit substrates, wherein both of the first and second conductive bumps are electrically coupled to a data input, a data output, and/or an address input of the third integrated circuit substrate wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates.

Claim 32 (canceled).

33. (previously presented) An electronic device according to Claim 31 wherein both of the first and second conductive bumps are electrically coupled to a data input, a data output, and/or an address input of the second integrated circuit substrate, and to a data input, a data output, and/or an address input of the first integrated circuit substrate.

34. (previously presented) An electronic device according to Claim 30 wherein the first, second, and third integrated circuit substrates are memory devices having a same layout.

35. (previously presented) An electronic device according to Claim 21 wherein the first and second ends of the second integrated circuit substrate comprise first and second opposing ends of the second integrated circuit substrate.

36. (previously presented) An electronic device according to Claim 21 wherein the

first, second, and third integrated circuit substrates have devices sides facing the printed circuit board and backsides facing away from the printed circuit board, the electronic device further comprising:

a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates;

a second conductive bump between the second and third integrated circuit substrates wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates;

a third conductive bump between the first integrated circuit substrate and the printed circuit board wherein the third conductive bump provides electrical and mechanical connection between the first integrated circuit substrate and the printed circuit board;

a fourth conductive bump between the second integrated circuit substrate and the printed circuit board wherein the fourth conductive bump provides electrical and mechanical connection between the second integrated circuit substrate and the printed circuit board; and

a fifth conductive bump between the second integrated circuit substrate and the first integrated circuit substrate wherein the fifth conductive bump provides electrical and mechanical connection between the first and second integrated circuit substrates.

37. (previously presented) An electronic device according to Claim 36 wherein the printed circuit board includes a first conductive pad to which the third conductive bump is bonded and a second conductive pad to which the fourth conductive bump is bonded, wherein the first conductive pad has a greater surface area than the second conductive pad.

38. (previously presented) An electronic device according to Claim 36 further comprising:

a first conductive trace on the printed circuit board providing electrical coupling between the third and fourth conductive bumps;

a second conductive trace on the second substrate providing electrical coupling

between the fourth and fifth conductive bumps; and

a third conductive trace on the first substrate providing electrical coupling between the fifth and first conductive bumps.

39. (previously presented) An electronic device according to Claim 38 wherein the first and third conductive bumps are electrically coupled to a data input, a data output, and/or an address input of the first substrate, and wherein the first and third conductive bumps are electrically coupled to a data input, a data output, and/or an address input of the third substrate.

40. (previously presented) An electronic device according to Claim 21 further comprising:

a fourth integrated circuit substrate on the third integrated circuit substrate wherein the third integrated circuit substrate is between the second and fourth integrated circuit substrates;

a fifth integrated circuit substrate on the fourth integrated circuit substrate wherein the fourth integrated circuit substrate is between the third and fifth integrated circuit substrates, wherein the fourth integrated circuit substrate is offset relative to the first, third, and fifth integrated circuit substrates so that the second end of the second integrated circuit substrate extends beyond the first, third, and fifth integrated circuit substrates, and so that the first, third, and fifth integrated circuit substrates extend beyond the fourth integrated circuit substrate.

Claim 41 (canceled).

42. (previously presented) An electronic device comprising:

a first integrated circuit substrate having opposing first and second surfaces;

a second integrated circuit substrate on the first integrated circuit substrate, the second integrated circuit substrate having opposing first and second surfaces;

a third integrated circuit substrate on the second integrated circuit substrate, the third integrated circuit substrate having opposing first and second surfaces, wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the first surface of the second integrated circuit substrate faces the second surface of the first integrated circuit substrate, and wherein the second surface of the second integrated circuit substrate faces the first surface of the third integrated circuit substrate; and

a signal path extending along a first conductive trace on the first surface of the second integrated circuit substrate, to the second surface of the first integrated circuit substrate, along a second conductive trace on the second surface of the first integrated circuit substrate, to the first surface of the third integrated circuit substrate, along a third conductive trace on the first surface of the third integrated circuit substrate, and to the second surface of the second integrated circuit substrate.

43. (previously presented) An electronic device according to Claim 42 wherein the signal path comprises a first conductive bump between the first surface of the second integrated circuit substrate and the second surface of the first integrated circuit substrate, a second conductive bump between the second surface of the first integrated circuit substrate and the first surface of the third integrated circuit substrate, and a third conductive bump between the first surface of the third integrated circuit substrate and the second surface of the second integrated circuit substrate.

44. (previously presented) An electronic device according to Claim 43 wherein wherein the first conductive bump provides electrical and mechanical connection between the first and second integrated circuit substrates, wherein the second conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates, and wherein the third conductive bump provides electrical and mechanical connection between the third and second integrated circuit substrates.

45. (previously presented) An electronic device according to Claim 42 wherein the

first side of the first and third integrated circuit substrates comprises a device side and wherein the second side of the first and third substrates comprises a backside.

46. (previously presented) An electronic device according to Claim 45 wherein the signal path is electrically coupled to an electronic circuit of the third integrated circuit substrate.

47. (previously presented) An electronic device according to Claim 45 wherein the first side of the second integrated circuit substrate comprises a device side and wherein the second side of the second integrated circuit substrate comprises a backside.

48. (previously presented) An electronic device according to Claim 47 wherein the signal path is electrically coupled to an electronic circuit of the second integrated circuit substrate and to an electronic circuit of the third integrated circuit substrate.

49. (previously presented) An electronic device according to Claim 47 wherein the first, second, and third integrated circuit substrates are respective integrated circuit memory devices.

50. (previously presented) An electronic device according to Claim 42 further comprising:

a fourth integrated circuit substrate on the third integrated circuit substrate wherein the third integrated circuit substrate is between the second and fourth integrated circuit substrates; and

wherein the signal path further extends along the second surface of the second integrated circuit substrate, and to a first surface of the fourth integrated circuit substrate.

51. (previously presented) An electronic device according to Claim 50 wherein the signal path is electrically coupled with electronic circuits of the second and fourth integrated

circuit substrates.

52. (previously presented) An electronic device comprising:

a first integrated circuit substrate having opposing first and second surfaces;

a second integrated circuit substrate on the first integrated circuit substrate, the second integrated circuit substrate having opposing first and second surfaces;

a third integrated circuit substrate on the second integrated circuit substrate, the third integrated circuit substrate having opposing first and second surfaces, wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;

a signal path extending along the first surface of the second integrated circuit substrate, to the second surface of the first integrated circuit substrate, along the second surface of the first integrated circuit substrate, to the first surface of the third integrated circuit substrate, along the first surface of the third integrated circuit substrate, and to the second surface of the second integrated circuit substrate; and

a fourth integrated circuit substrate on the third integrated circuit substrate wherein the third integrated circuit substrate is between the second and fourth integrated circuit substrates; and

wherein the signal path further extends along the second surface of the second integrated circuit substrate, and to a first surface of the fourth integrated circuit substrate;

wherein the signal path is electrically coupled directly with an electronic circuit of the fourth integrated circuit substrate, and wherein the signal path is free of direct electrical coupling with any electronic circuit of the second integrated circuit substrate.

Claims 53-54 (canceled).

55. (previously presented) An electronic device according to Claim 59 wherein the first array of interconnection structures comprises an array of interconnection bumps and wherein the second array of interconnection structures comprises an array of conductive pads free of interconnection bumps.

56. (original) An electronic device according to Claim 55 wherein the interconnection bumps comprise solder bumps and wherein the conductive pads comprise solder wettable pads.

57. (previously presented) An electronic device according to Claim 59 further comprising:

a third array of interconnection structures on the first surface of the substrate spaced apart from the first array of interconnection structures wherein the third array of interconnection structures are arranged in a third pattern;

a fourth array of interconnection structures on the second surface of the substrate spaced apart from the second array of interconnection structures wherein the fourth array of interconnection structures are arranged in a fourth pattern, wherein the fourth pattern is a mirror image of the third pattern.

58. (original) An electronic device according to Claim 57 further comprising:

a first plurality of conductive traces on the first surface of the substrate wherein the first plurality of conductive traces provide interconnection between at least some of the interconnection structures of the first and second arrays on a one to one basis.

59. (previously presented) An electronic device comprising:

a substrate having opposing first and second surfaces;

a first array of interconnection structures on the first surface of the substrate wherein the first array of interconnection structures are arranged in a first pattern;

a second array of interconnection structures on the second surface of the substrate wherein the second array of interconnection structures are arranged in a second pattern and wherein the second pattern is a mirror image of the first pattern wherein the substrate comprises an integrated circuit substrate such that the first surface is a device side of the substrate having electronic circuits thereon and the second surface is a backside of the

substrate.

60. (previously presented) An electronic device according to Claim 59 wherein the integrated circuit substrate is an integrated circuit memory device.

61. (canceled).

62. (previously presented) An electronic device according to Claim 12 wherein each of the first, second, and third integrated circuit substrates comprises a rectangular substrate having a length and a width such that the lengths and the widths of each of the first, second, and third integrated circuit substrates are the same, and wherein lengthwise directions of each of the first, second, and third integrated circuit substrates are arranged in parallel.

63. (previously presented) An electronic device according to Claim 59 wherein the backside of the substrate is free of electronic circuits.

64. (previously presented) An electronic device according to Claim 7 wherein each of the first, second, and third integrated circuit substrates has a same length and width.

65. (previously presented) An electronic device according to Claim 7 wherein each of the first, second, and third integrated circuit substrates is an integrated circuit memory device.

66. (previously presented) An electronic device according to Claim 15 wherein the fourth conductive bump is spaced apart from and extends past an edge of the first integrated circuit substrate

67. (previously presented) An electronic device according to Claim 19 wherein the first, second, third, fourth, and fifth integrated circuit substrates have

device sides facing a first direction and backsides facing a second direction.

68. (previously presented) An electronic device according to Claim 7 wherein each of the first, second, and third integrated circuit substrates is a semiconductor integrated circuit substrate.

69. (previously presented) An electronic device according to Claim 9 wherein each of the first, second, and third integrated circuit substrates is a semiconductor integrated circuit substrate.

70. (previously presented) An electronic device according to Claim 15 wherein each of the first, second, and third integrated circuit substrates is a semiconductor integrated circuit substrate.

71. (previously presented) An electronic device according to Claim 19 wherein each of the first, second, third, fourth, and fifth integrated circuit substrates is a semiconductor integrated circuit substrate.

72. (previously presented) An electronic device according to Claim 23 wherein each of the first, second, and third integrated circuit substrates is a semiconductor integrated circuit substrate.

73. (previously presented) An electronic device according to Claim 27 wherein each of the first, second, and third integrated circuit substrates is a semiconductor integrated circuit substrate and wherein the first conductive bump is connected between portions of the first and third semiconductor integrated circuit substrates that extend beyond the end of the second semiconductor integrated circuit substrate.

74. (previously presented) An electronic device according to Claim 59 wherein the

substrate is a semiconductor integrated circuit substrate.

75. (previously presented) An electronic assembly comprising:

a first integrated circuit substrate;

a second integrated circuit substrate on the first integrated circuit substrate; and

a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond a first end of the second integrated circuit substrate wherein a second end of the second integrated circuit substrate extends beyond the first and third integrated circuit substrates wherein the first, second, and third integrated circuit substrates are configured to be mounted on a same side of a printed circuit board so that device sides of the first, second, and third integrated circuit substrates face the printed circuit board and so that backsides of the first, second, and third integrated circuit substrates face away from the printed circuit board.

76. (previously presented) An electronic assembly according to Claim 75 further comprising:

a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates; and

a second conductive bump between the second and third integrated circuit substrates wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates.

77. (previously presented) An electronic assembly according to Claim 76 wherein the first, second, and third integrated circuit substrates have a same size.

78. (previously presented) An electronic assembly according to Claim 76 wherein the

first conductive bump is between portions of the first and third integrated circuit substrates extending beyond the end of the second integrated circuit substrate.

79. (previously presented) An electronic assembly according to Claim 76 further comprising:

a conductive trace on a surface of the third integrated circuit substrate, the conductive trace providing an electrical coupling between the first and second conductive bumps.